VELAMMAL INSTITUTE OF TECHNOLOGY, CHENNAI- 601204
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
EC 6602 VLSI DESIGN 06 SEMESTER ECE

QUESTION BANK

UNIT I

1. Explain the electrical properties of CMOS/Derive the equation for source to drain current (I_{ds}) in different operating regions of a MOS transistor and also draw the VI characteristics
2. Explain briefly about Second order I-V Effects of MOS Transistors/Explain body effect and its effect in MOS
3. Explain the DC Transfer characteristics of a CMOS inverter with necessary conditions for different regions of operation
4. Explain in detail about the scaling concept and its fundamental limits.
5. Explain the Layout design rules and draw the Layout for CMOS inverter/4 input NAND/NOR
6. Explain the different steps involved in n well CMOS fabrication process
7. Discuss the mathematical equations that can be used to model the drain current and diffusion capacitance of MOS transistor. Also derive the noise margin for a CMOS inverter.

UNIT II

1. Draw the CMOS logic circuit for the following expression and explain:Z=[A(B+C)+DE]'. Draw the static CMOS logic circuit for the following expression: (i) Y= [A.B.C.D]' and (ii) Y=[D(A+BC)]'
2. Explain the basic principle of transmission gate in CMOS design/Discuss in detail the characteristics of CMOS transmission gate/ Explain the use/application of transmission gate.
3. Explain in detail about DCVSL logic with suitable example. Explain the operation of domino and dual-rail domino in dynamic circuits
4. Discuss the various types of power dissipation and also explain the methods to reduce the switching activity in static and dynamic CMOS circuits. / Explain static and dynamic power dissipation in CMOS circuits/Discuss the low power design principles

in detail / What are the sources of power dissipation in CMOS and discuss various design techniques to reduce power dissipation in CMOS

5. Write short notes on ratioed circuits and dynamic CMOS circuits
6. Explain the operation of domino and dual-rail domino in dynamic circuits
7. Explain the Techniques to tackle large fan in
8. Discuss the static properties, Propagation delay calculation and control using transistor resizing
9. With an example explain Elmore delay model
10. Explain delay calculation using logical effort.

UNIT III

1. Design and analyze the master-slave based edge triggered register using transmission gates/ Explain the operation of master-slave based edge triggered register
2. How the TSPCR eliminate the race around problem in sequential circuit? / Explain the operation of true single phase clock registers
3. Discuss in detail various static latches and registers
4. Explain how the C^2MOS Register provides race free sequential circuit with neat diagram/Explain NORA CMOS circuits
5. Discuss any one dynamic register and latches in sequential circuit
6. Explain how the pipelining technique improves the performance in sequential circuit. / Discuss about the design of sequential dynamic circuits and its pipelining concept/ Discuss in detail various pipelining approaches to optimize sequential circuits
7. Explain the timing basics and clock distribution techniques in synchronous design in detail/Explain the concept of timing issues.
8. Draw and explain the operation of conventional, pulsed and resettable latches.

UNIT IV

1. Draw the structure of ripple carry adder and explain its operation. Discuss how the drawback of ripple carry adder is overcome by carry look ahead adder/ Explain the concept of carry look ahead adder and discuss its speed-area trade off/ Explain the operation of a basic 4 bit adder and describe the different approaches of improving the speed of the adder.

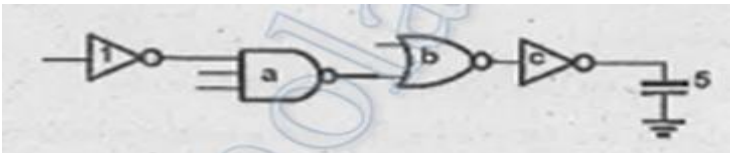
2. Explain about carry bypass adder and carry select adder/ Discuss a 16 bit carry bypass/carry skip and carry select adder & discuss their features
3. Explain about accumulators, dividers, Barrel shifters
4. Discuss a 4x4 array multiplier and write down the equation for delay.
5. Explain the concept of modified Booth multiplier with a suitable example/ Explain the operation of Booth multiplication with suitable examples. Justify how Booth's algorithm speeds up the multiplication process.
6. Explain about Wallace tree multiplier

UNIT V

1. Explain the different types of ASIC with neat diagram/Write short notes on full custom ASIC and semi custom ASIC
2. Explain the architecture of FPGA. / Draw and explain the building blocks of FPGA architecture/Draw the Xilinx XC4000 CLB and explain the operation
3. Explain about CLB, IOB and programmable interconnect of Xilinx FPGA device.
4. Draw and explain the operation of ACTEL FPGA modules with neat diagram
5. Write short notes on routing procedures involved in FPGA interconnect
6. Discuss the different types of programming technology used in FPGA design

PART C

1. Estimate the least delay and determine the input capacitance of each stage for the logic network shown in fig., which may represent the critical path of a more complex logic block. The output of the network is loaded with a capacitance which is 5 times larger than the input capacitance of the first gate which is a minimum sized inverter.



2. Consider the circuit shown in figure 1.

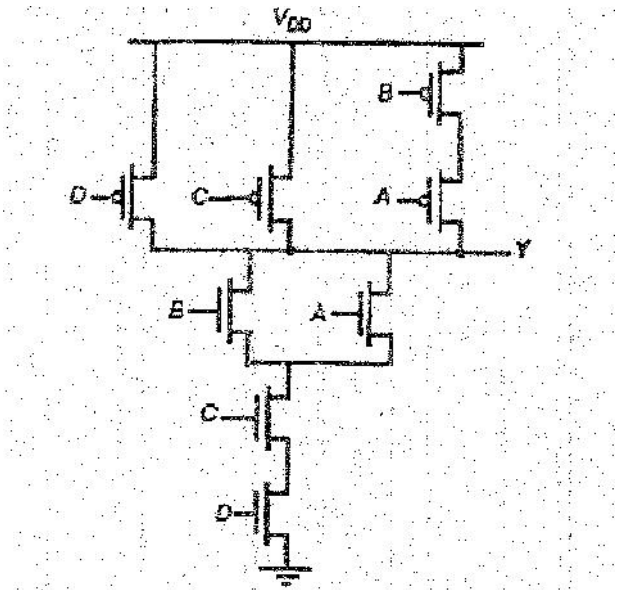
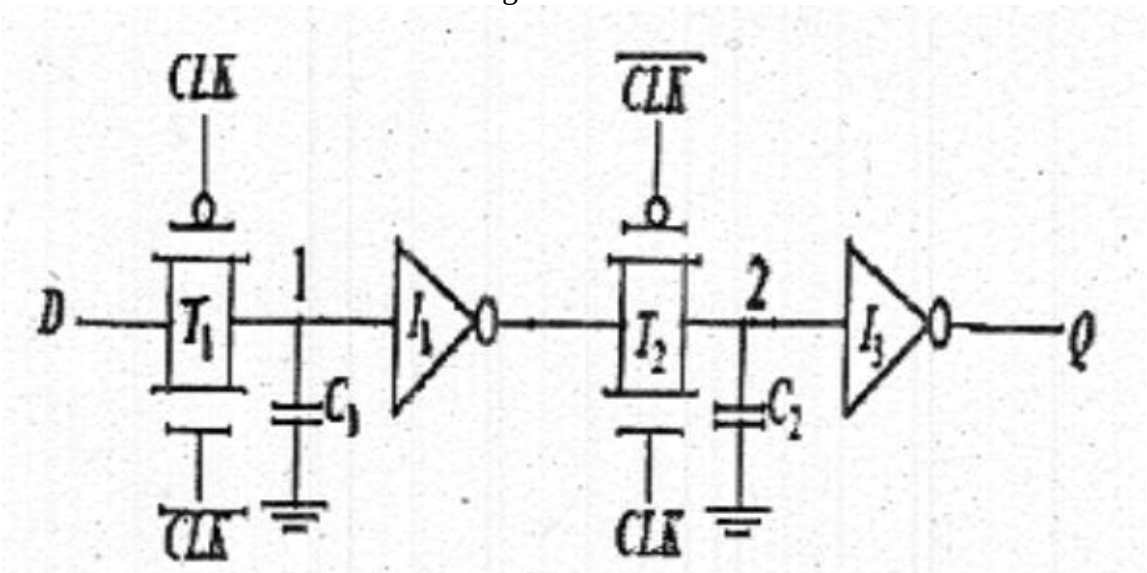


Figure 1

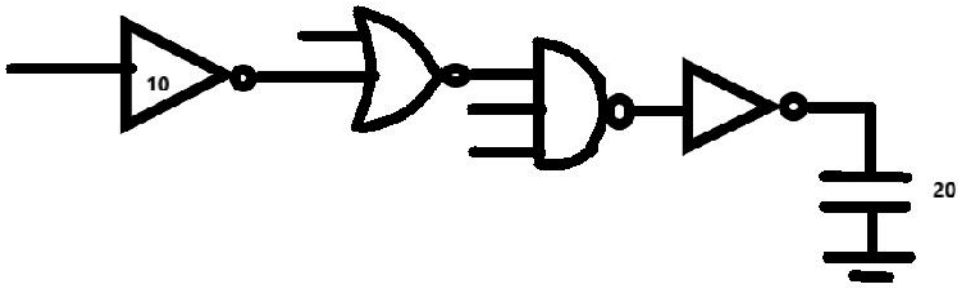
(i) What is the logic function implemented by the CMOS transistor network? (5)
(ii) Realize the above network using pseudo nmos logic. (5)
(iii)Compare the two networks and Comment your observations. (5)

3. Consider the circuit shown in figure:



(i) State whether the circuit is a latch or an edge triggered register. Justify your answer. (7)
In the circuit consider C1 and C2 as the intrinsic capacitances of inverter and transmission gates. Assuming ideal clock, compute the setup time and hold time. (8)

4. Calculate the path logical effort, path effort, and gate effort for the given circuit:

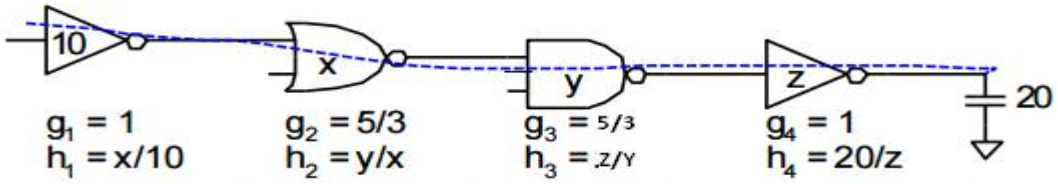


Logical effort generalizes to multistage networks

Path Logical Effort $G = \prod g_i$

Path Electrical Effort $H = \frac{C_{\text{out-path}}}{C_{\text{in-path}}}$

Path Effort $F = \prod f_i = \prod g_i h_i$



PATH LOGICAL EFFORT, G=(1) X (5/3) X (5/3) X (1)=25/9 --→ (5) marks

PATH ELECTRICAL EFFORT, H=20/10=2 --→ (5) marks

PATH EFFORT, F=G.H=(25/9)X2=50/9 --→ (5) marks

5. Design a multiplier for 5 bit by 3 bit using Wallace tree structure. Explain its operation and summarize the number of adders used
6. What are non ideal clocks? Explain with an example. Design a circuit to generate non overlapping clocks
7. Implement Half Adder using complementary CMOS logic
8. Briefly discuss λ based design rules and sketch the layout of 4 input NAND gate and 3 input AND gate.